E1: Dual-Chamber Pacemaker Synchronization Using Galvanic Intrabody Communication

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Introduction

Effective cardiac function requires coordinated pacing across multiple heart chambers — especially in patients with arrhythmias or heart failure.

Leaded Pacemakers

Advantages: Provide coordination

Disadvantages:

- Involve **invasive procedures**
- Risks like **lead failure**, **infection**, **lead dislodgement.**

Leadless Cardiac Pacemakers

Advantages: Minimally invasive

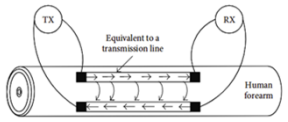
Disadvantages:

- **Not built for synchronization**
- Consume **high power**.

Background

Galvanic Intrabody Communication (IBC)

- Uses the human body as the transmission medium.
- Enables low-power, low-frequency communication between implanted devices.
- Offers high reliability with minimal energy consumption.



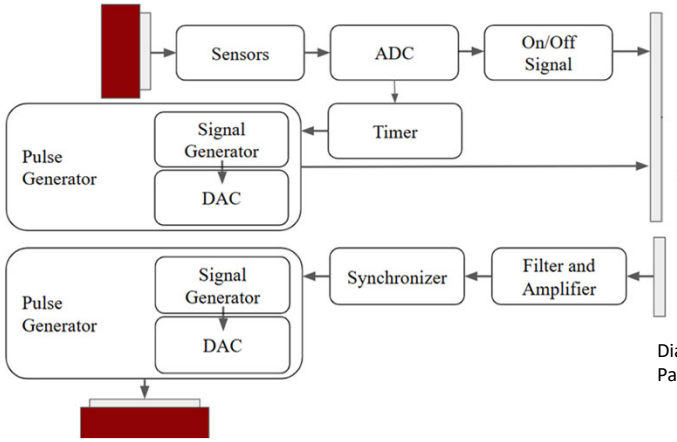
Opportunity

- Combining Galvanic IBC with leadless pacemakers enables synchronized multi-node cardiac pacing.
- Enhances therapeutic outcomes while preserving a minimally invasive approach.

Challenges and Approach

Problem	Solution Approach
Synchronize reliably across devices in the presence of tissue attenuation and noise	Design low-energy, tissue-safe communication signals
Minimize energy consumption to extend pacemaker life	Implement noise mitigation and error correction
Ensure biocompatibility and avoid unintended stimulation	Develop precise timing schema for synchronization
Scale communication to multi-node systems without crosstalk	Create scalable, collision-free multi-device protocols
Meet FDA and FCC regulatory standards	Validate performance against medical communication regulations

System Overview



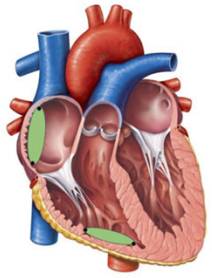
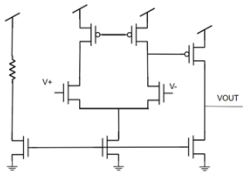


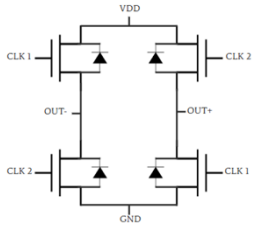
Diagram of Heart with Pacemakers Positioned

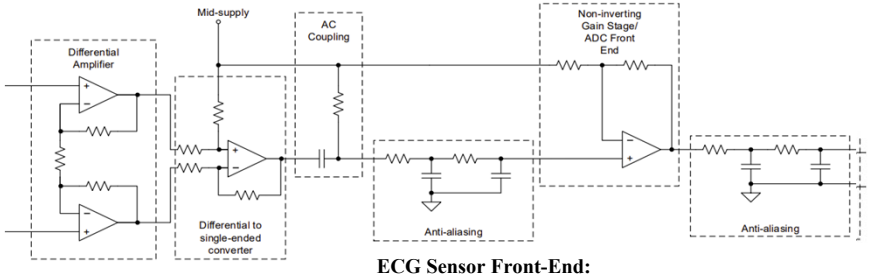
CMOS Circuit Design Specifications

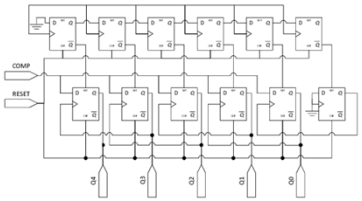


Operational Transconductance Amplifier (OTA):
Converts an input voltage difference into an output current. Commonly used in analog systems such as filters, amplifiers, and data converters.

Clock Pulse Generator:
A differential circuit that produces complementary outputs (OUT+ and OUT−) based on two non-overlapping clock signals (CLK1 and CLK2).



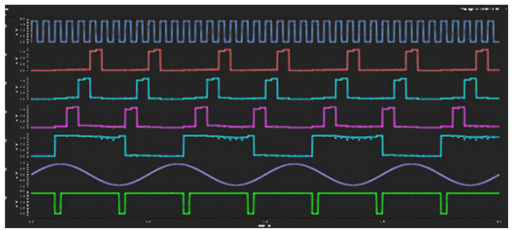




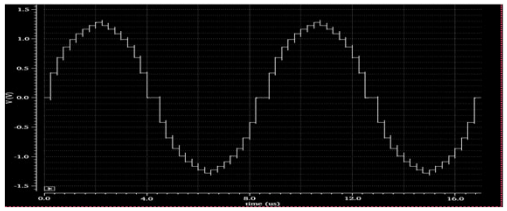
ECG Sensor Front-End:
Amplifies the differential ECG signal, removes DC offsets through AC coupling, filters out high-frequency noise with anti-aliasing stages, and prepares the signal with appropriate gain for analog-to-digital conversion.

Successive Approximation Register (SAR) ADC Logic:
Uses D flip-flops to store and shift comparison results from the comparator (COMP input), progressively refining the digital output (Q4 to Q0) with each clock cycle. The RESET signal initializes the system before each conversion cycle.

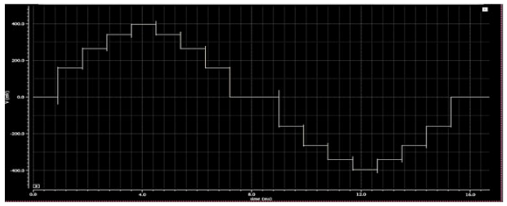
Simulation Results



Simulation of Sensor and Analog to Digital Conversion



Simulation of Synchronization Signal



Simulation of Pacemaker Signal

Conclusions

- Developed strategies to achieve reliable, low-power synchronization of leadless cardiac pacemakers.
- Designed scalable, biocompatible communication protocols that meet regulatory standards.
- Results support future multi-node cardiac therapies with improved safety and efficiency.

Future Work

- Complete full chip layout, optimizing area and power.
- Successfully prepared the design for tapeout, enabling future multi-node pacemaker integration.

References

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